Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – WINTER 2012

Subject code: 715205 Date: 12-01-2013

Subject Name: Advanced Computer Architecture

Time: 02.30 pm – 05.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** What are the two key metrics of computer architecture? **07**

(b) How does download/upload bandwidth impact the performance of a webinar session? Overall, how accurate is a result from speedtest.net at determining the quality of a webinar experience? **07**

Q.2 **(a)** The new Nikon D7000 camera is retailing in the market for around INR 31,000. Speculate and draw a sample block diagram of its internals. **07**

(b) What is the possible BOM cost of the above device? Base your answer on what the average profitability seen in class was. **07**

OR

(b) Assume that the ping is decreased from 250ms to 50ms. What effect does this have on a webinar session conducted in the global class room? **07**

Q.3 **(a)** Draw a pipeline diagram for the following instructions: **07**
Instructions are in the format <op> <source 1> <source2> <dest>

```
L1:  ADD A B C
     MUL A B X
     BEQ X 2 L1
     SUB E F G
     OR E H K
```

(b) What is the need for pipelining architecture? Give examples of non-pipelined and pipelined architecture being used in the embedded systems market. **07**

OR

Q.3 **(a)** What is a TLB? How does it improve system performance and why? **07**

(b) How does a set-associative cache work? Explain with an example. In which cases is it preferred over the fully-associative cache? **07**

Q.4 **(a)** What is a benchmark? If you were buying a PC for your parents how would you use the numbers on that platform for SpecInt, Specfp and TPC-C? **07**

(b) What is the bandwidth required to do a two way video conference at 1600x1200 pixels, 8 bit Truecolor? **07**

OR

Q.4 **(a)** A processor receives an NMI from a temperature sensor on the board.. The processor is in the EX stage of an instruction. Should the processor jump to the ISR right away or wait till the instruction finishes? What are the hazards of an interrupt being serviced in the middle of an instruction? **07**

(b) For each of the following classes of computer which architecture would you **07**

choose – homogenous or heterogeneous multiprocessors? Justify your answer.

a) Fiber optic network Packet processor

b) Digital Television

c) DSP processor

d) Digital Camcorder

Q.5	**(a)**	The AMD Processor has a 64 bit address. If a laptop has 4GB RAM, 320GB hard drive, of which 100GB is swap space and the file system is organized to have 4KB size pages, how many pages are available?	**07**
	(b)	What is the impact of a page fault? Use a picture or flow diagram if needed	**07**

OR

Q.5	**(a)**	In which cases/scenario is a write-through cache preferred over a write-back cache. Justify your answer with an example.	**07**
	(b)	What is the time taken for a 1MB file PCI to USB transfer? Assume PCI-33MHz, 32bit bus and serial data USB 1.0. USB 1.0 runs at 48Mbps.	**07**

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