

GUJARAT TECHNOLOGICAL UNIVERSITY
M. E. - SEMESTER – II • EXAMINATION – WINTER 2012

Subject code: 725201**Date: 29-12-2012****Subject Name: Digital VLSI Design II - Backend****Time: 10.30 am – 01.00 pm****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) In the typical ASIC flow, explain the importance of Physical Design & different steps associated it. **07**
- (b) What is metastability? When does it occur? What happens to a 4 bit free running counter if it enters metastability? **07**

- Q.2** (a) Explain the following commands **07**
- A. Compile used in DC
 - B. Initialize_floorplan used in ICC
 - C. Create_mw_lib used in ICC
- (b) Explain the following terms **07**
- D. Setup violation
 - E. Hold violation
 - F. Clock Skew

OR

- (b) Tabulate the differences between ddc & verilog netlist formats. **07**

- Q.3** (a) Differentiate the Floor planning process associated with design of a simple FSM & a Protocol with Macro. **07**
- (b) What are logical & physical libraries? Where are they used & how do they differ from each other? **07**

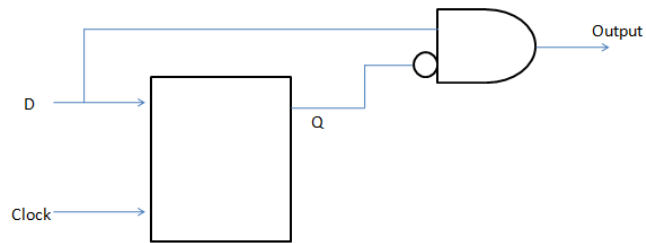
OR

- Q.3** (a) What is the difference between timing calculations achieved using Wireload models during synthesis process & timing calculations after place & route for a digital circuit? **07**
- (b) A chip is said to be Timing & Power critical. What steps can be taken to achieve these specifications? **07**

- Q.4** (a) What is clock tree synthesis & optimization? Why is it important in Digital IC design flow? **07**
- (b) Explain clock_opt command with any 2 options available with it **07**

OR

- Q.4** (a) Mention any 3 different types of violations possible during Synthesis or PD process & briefly explain them **07**
- (b) Draw the timing diagram of the circuit for 110001101 input sequence **07**



- Q.5 (a)** Explain the following terms **07**
- A. Negative slack
 - B. Clock Jitter
 - C. Critical Path
 - D. False Path

- (b)** Explain the importance of different metal layers for use in PD flow? **07**

OR

- Q.5 (a)** Design a controlled inverter circuit & draw the stick diagram for the same **07**
 (You can invert input / send the same as output at will!!)
- (b)** A design has been synthesized for 300MHz. However, after place and route, the results of Primetime indicate that there are timing violations. The WNS is -0.4ns and the TNS is -1.2ns. What is the frequency that this design can run at now, if we were to ignore this violation and send the design for fabrication? **07**
