Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – WINTER • 2013

Subject code: 1722602 Date: 27-12-2013

Subject Name: CMOS Circuit Design - II

Time: 10.30 am – 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw multiply-by-two SC circuit. What should be sequence of operation of switches and why? Also draw its equivalent circuits for sampling and amplification phases.	**07**
	(b)	Draw switched-capacitor (SC) unity gain buffer circuit which has three switches. What should be the sequence of operation of switches to minimize the error? Justify your answer. Derive expression for precision of this circuit.	**07**
Q.2	**(a)**	In a self-bias voltage reference circuit with resistor biasing, derive the dependence of output current on output resistance of each transistor in the circuit.	**07**
	(b)	How does the op-amp input offset voltage affect the output voltage in temperature independent voltage reference circuit? What are the solutions to solve this problem? Draw the final circuit which has the less effect of op-amp input offset voltage.	**07**
		OR	
	(b)	Show with appropriate reference generator circuit that the output noise is approximately same as input-referred noise voltage of op amp.	**07**
Q.3	**(a)**	What will be the effect of unequal charging and discharging current in basic charge pump PLL on its operation? Explain with necessary waveforms.	**07**
	(b)	Draw loop gain characteristics of simple charge pump PLL with and without R in series of C. Discuss the effect of R on stability of the circuit. Derive transfer functions of simple charge pump PLL with R in series of C.	**07**
		OR	
Q.3	**(a)**	Derive transfer function of simple PLL and discuss trade-off between various parameters to improve its performance.	**07**
	(b)	Can we have zero phase error in basic charge pump PLL? Justify your answer with necessary waveforms and comments.	**07**
Q.4	**(a)**	Draw and explain the block diagram of voltage comparator. Discuss the operation of positive feedback decision circuit with necessary equations in detail.	**07**
	(b)	Explain the basic charge pump concept to generate positive voltage greater than V_{DD}.	**07**
		OR	
Q.4	**(a)**	What are the different performance parameters of voltage comparator? Explain in brief how would you measure each of them with diagrams and waveforms?	**07**
	(b)	Explain working of one of the serial ADCs.	**07**

Q.5 **(a)** Explain the principle of chopper stabilization used to reduce effects of 1/*f* noise and input-offset voltage. Also explain that how it can be included in CMOS op-amp. **07**

(b) Draw circuit schematic of sense amplifier which has rail-to-rail input range, minimum kick-back noise and "no memory." Discuss its working and justify that it has above mentioned features. **07**

OR

Q.5 **(a)** What are the issues to be considered in the design of sense amplifier? Draw basic sense amplifier and explain its working. **07**

(b) Draw commonly used differential input stage and derive expression for minimum value of V_{DD} such that all transistors are ON and operating in saturation region. Also derive expressions for ICMR (input common mode range) for the same circuit for a particular value of V_{DD}. Draw parallel n-channel and p-channel differential stage and write expressions for its ICMR. **07**

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