Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – WINTER • 2014

Subject code: 1724202 Date: 03-12-2014

Subject Name: Testing and Verification of VLSI Design

Time: 02:30 pm - 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Give the comparison between verification and testing.	**07**
	(b)	Explain the following terms with respect to Testing. I. Test Specification. II. Test Plan.	**07**
Q.2	**(a)**	Explain the following terms with respect to Test economics. I. Defining Cost. II. Production.	**07**
	(b)	Explain the Scan Based testing.	**07**
		OR	
	(b)	What is linking tool? Explain in detail.	**07**
Q.3	**(a)**	What is the importance of Verification? Explain in detail.	**07**
	(b)	Explain the following terms with respect to verification. I. Design Reuse. II. Verification Reuse.	**07**
		OR	
Q.3	**(a)**	Explain the single stuck-at fault with example.	**07**
	(b)	What is the difference between Simulator and Emulator?	**07**
Q.4	**(a)**	What is functional verification? Explain in detail	**07**
	(b)	Explain the role of testing.	**07**
		OR	
Q.4	**(a)**	What is the signification of fault coverage? Explain in detail.	**07**
	(b)	Explain in the following terms. I. Fault Modeling. II. Fault Dominance. III. Pattern sensitive faults.	**07**
Q.5	**(a)**	Explain the VLSI realization process with necessary figures.	**07**
	(b)	Write a short note on Testing Philosophy.	**07**
		OR	
Q.5	**(a)**	Compare the online BIST and Offline BIST	**07**
	(b)	List the different types of Ad hoc DFT techniques and explain any four.	**07**

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