

GUJARAT TECHNOLOGICAL UNIVERSITY
ME - SEMESTER- I • EXAMINATION – WINTER 2014

Subject Code: 2712602**Date: 07/01/ 2015****Subject Name: CMOS CIRCUIT DESIGN-I****Time: 02:30 p.m. to 05:00 p.m.****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

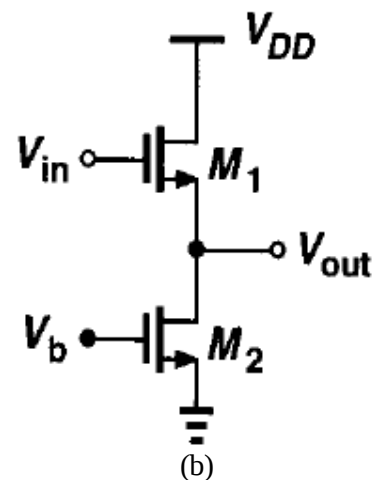
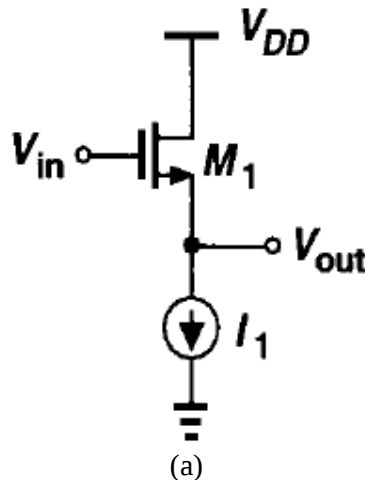
Q.1 (a) Do as Directed:**07**

- (i) Draw the short circuit current waveform in CMOS inverter, in case of dissipation due to direct-path current, with finite rise and fall time input waveform.
- (ii) Write the delay equation of an N-bit adder, when adder is divided in (N/M) equal-length bypass stages, each of which contains M bits.
- (iii) Write any two MOSFET transconductance equations.
- (iv) Explain shielding property of Cascode amplifier.
- (v) Describe advantage of differential amplifier operation over single-ended amplifier operation.
- (vi) Discuss Large signal bandwidth in operational amplifier.
- (vii) In which region of operation MOS device can act as a current source? Why?

(b) In source follower, as shown in figure (a), $(W/L)_1 = 20/0.5$, $I_1 = 200$ micro Ampere, $V_{TH0} = 0.6$ V, $2\phi_F = 0.7$ V, $\mu_n C_{ox} = 50$ microAmpere/V², and $\gamma = 0.4$ V^{1/2}, **07**

(I) Calculate V_{out} for $V_{in} = 1.2$ Volt

(II) If I_1 is implemented as M_2 in figure (b), find the maximum value of $(W/L)_2$ for which M_2 remains saturated.



Q.2 (a) Derive voltage gain A_v and output resistance R_{out} for Source follower. **07**

(b) Discuss Method I of Quantitative analysis of differential pair. **07**

OR

(b) Discuss Linear Carry Select Adder for 4 bit as well as 16 bit. Also show critical path in gray shad in 16 bit adder block diagram. **07**

Q.3 (a) Discuss CS stage with source degeneration and derive R_{out} . **07**

(b) Write expression for total power consumption in CMOS inverter and explain static power consumption. **07**

OR

Q.3 (a) How to construct a differential pair whose gain is varied by a control voltage? Discuss Gilbert **07**

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- (b) Discuss Active current mirrors in brief. **07**
- Q.4** (a) Draw high frequency model of Common Gate stage and explain. **07**
- (b) Draw, discuss and compare simple op-amp topologies and Cascode op amps. **07**
- OR**
- Q.4** (a) Explain in detail slew rate in op-amp. **07**
- (b) Draw bode plots of loop gain for unstable and stable systems and discuss Multipole Systems. **07**
- Q.5** (a) Discuss Dynamic Threshold Scaling (DTS). **07**
- (b) Discuss following: **07**
- (I) Channel-Length Modulation
- (II) Reducing the power in standby (or Sleep) Mode.
- OR**
- Q.5** (a) Explain the following: **07**
- (1) Basics of current mirror
- (2) Noise Margin
- (b) Discuss 4x4 Carry Save Multiplier with critical path is highlighted in gray in block diagram. **07**
