Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– • EXAMINATION – WINTER 2014

Subject Code: 2735201 **Date: 25-11-2014**

Subject Name: Design for Test

Time: 2:30 P.M. – 5:00 P.M. **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain Mux Flip-flop scan architecture and its operation in different mode.	**07**
	(b)	Explain memory BIST operation with block diagram.	**07**
Q.2	**(a)**	Write down about stuck-at-fault model in detail.	**07**
	(b)	Explain JTAG architecture in detail with all JTAG pins.	**07**
		OR	
	(b)	What is TAP state machine? Explain with state diagram.	**07**
Q.3	**(a)**	Write down short note on: A. Difference between Transition delay fault (TDF) model and Path delay fault (PDF) model. B. IDDQ test.	**04+03**
	(b)	Explain following untestable faults: A. Unused B. Tied C. Blocked D. Redundant	**07**
		OR	
Q.3	**(a)**	Write down short note on: A. Difference between parametric test and functional test. B. What are Defect, Error and Fault?	**04+03**
	(b)	Explain following testable faults: A. Possible detected B. ATPG untestable	**07**
Q.4	**(a)**	What is LFSR and its use? Explain the structure of standard LFSR and modular LFSR.	**07**
	(b)	Explain following register used in Boundary scan architecture with its instruction. A. Bypass register B. Device Identification register	**07**
		OR	
Q.4	**(a)**	What is ATPG and its use? Explain ATPG concept with fault activation, fault propagation & line justification.	**07**
	(b)	Explain Boundary scan register with schematic?	**07**

Q.5 **(a)** Explain March-C algorithm with all steps used for MBIST. **07**

(b) A. What is Test coverage and Fault coverage? **04+03**

B. Find out the Test coverage and Fault coverage value with the help of below mentioned pattern generation Summary

fault class	code	#faults
Detected	DT	1200
detected_by_simulation	DS	(700)
detected_by_implication	DI	(500)
Possibly detected	PD	0
ATPG untestable	AU	120
Undetectable	UD	180
not-controlled	UC	(100)
not-observed	UO	(80)
Untestable		300
Unused	UU	(40)
Tied	TI	(30)
Blocked	BL	(70)
Redundant	RE	(120)
total faults		1800

OR

Q.5 **(a)** Write down short summary on: **06+01**

A. Below mentioned memory fault types-
Neighborhood pattern sensitive faults, Address decoder faults and Retention faults (RF)

B. What is Built-In-Self-Repair (BISR)?

(b) Explain scan chain operation for delay test with timing diagram on Launch on capture (LOC) and Launch on shift (LOS). **07**

****