

Seat No.: _____
No. _____

Enrolment

GUJARAT TECHNOLOGICAL UNIVERSITY
M. E. - SEMESTER – I • EXAMINATION – WINTER • 2014

Subject code: 710403N

Date: 03-12-2014

Subject Name: ASIC Design

Time: 10:30 am - 01:00 pm

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) What is CPLD? Draw its basic structure and give its applications. **07**
(b) Explain the ASIC Design flow. **07**
- Q.2** (a) How Look Up Table (LUT) is used to implement any function in FPGA? **07**
Explain with example.
(b) Explain assertion statement with example. **07**
- OR**
- (b) Explain the Floor Planning in detail. **07**
- Q.3** (a) What are the draw backs of PLAs? How PLAs are used to implement **07**
combinational circuits?
(b) Write a short note on Block statement and explain its applications. **07**
- OR**
- Q.3** (a) Write a short note on FPGA programming technologies. **07**
(b) Explain the conditional signal assignment statement and selected signal **07**
assignment statement with example.
- Q.4** (a) Explain Test Bench with example. **07**
(b) Briefly explain Finite State Machine (FSM) and write the advantages of Finite **07**
State Machine.
- OR**
- Q.4** (a) Explain configuration and package declaration statements using necessary **07**
examples.
(b) Briefly explain (i) Full Custom ASICs (ii) Standard Cell Based ASICs **07**
(iii) Gate-Array Based ASICs.
- Q.5** (a) Write a VHDL code for 4 bit Parallel adder using structural modeling style **07**
with neat circuit Diagram and Truth Table.
(b) Write a VHDL code for 16 input priority encoder with Truth Table. **07**
- OR**
- Q.5** (a) Write a VHDL code for 4x1 MUX using Behavioral and Dataflow modeling **07**
style.
(b) Write a VHDL code for 16 bit serial-in, serial-out shift register with inputs SI **07**
(serial input), RST (reset), EN (enable), CK (clock) and output SO (serial
output).
