

Seat No.: _____
No. _____

Enrolment

GUJARAT TECHNOLOGICAL UNIVERSITY
M. E. - SEMESTER – I • EXAMINATION – WINTER • 2014

Subject code: 710412N

Date: 08-12-2014

Subject Name: Digital VLSI Design

Time: 10:30 am - 01:00 pm

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) Write a short note on Device Isolation Techniques. **07**
(b) The CMOS n-Well process. **07**
- Q.2** (a) Explain Y-chart in detail. **07**
(b) Explain MOS structure with energy band diagram. **07**
- OR**
- (b) Derive expression for threshold voltage of MOS transistor. **07**
- Q.3** (a) Short note on Constant Field Scaling. **07**
(b) Write note on CPLD. **07**
- OR**
- Q.3** (a) Constant Voltage Scaling. **07**
(b) Write a Note on FPGA. **07**
- Q.4** (a) For a resistive load inverter with $V_{DD} = 5V$, $k'_n = 20\mu A/V^2$, $V_{T0} = 0.8 V$, $R_L = 200K\Omega$, and $W/L = 2$, Calculate the critical voltages on VTC and draw. Also find Noise Margin of the circuit. **07**
(b) Derive the switching threshold (V_{th}) for CMOS inverter. **07**
- OR**
- Q.4** (a) What is clock skew problem for NP-Domino CMOS Logic circuits? Explain True Single Phase Clock (TSPC) Dynamic CMOS Logic circuits. **07**
(b) Write a short note on Pre-discharge and Evaluate logic for dynamic logic circuits. **07**
- Q.5** (a) Explain in detail CMOS NOR2 gate. **07**
(b) Write a short note on C-MOS ring oscillator. Also derive expression for frequency of oscillations. **07**
- OR**
- (a) Explain in detail CMOS NAND2 gate. **07**
(b) Define delay time definitions for a CMOS inverter. **07**
