Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – III • EXAMINATION – WINTER • 2014

Subject code: 732604 Date: 27-11-2014

Subject Name: Low - Power CMOS VLSI Circuit Design

Time: 02:30 pm - 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw the generic structure of a Multiple Threshold CMOS (MTCMOS) circuits and explain MTCMOS circuits.	**07**
	(b)	List the three causes of power consumption and explain any one in detail.	**07**
Q.2	**(a)**	Explain the following terms in brief: 1. DIBL 2. Fowler-Nordheim tunneling	**07**
	(b)	List circuit techniques for leakage power reduction and explain any one in brief.	**07**
		OR	
	(b)	Discuss parallel processing approach in detail.	**07**
Q.3	**(a)**	Discuss Manchester Carry Chain and Manchester adder.	**07**
	(b)	Draw a 16 bit carry skip adder with 4-bit skip blocks.	**07**
		OR	
Q.3	**(a)**	Discuss EEPROM with its basic cell.	**07**
	(b)	Discuss Low power techniques at architecture level for ROM.	**07**
Q.4	**(a)**	Draw 4x4 bit Braun multiplier and explain it.	**07**
	(b)	Draw block diagram of an n x n-bit modified Booth multiplier and discuss modified booth multiplier.	**07**
		OR	
Q.4	**(a)**	Draw SRAM Architecture and discuss READ cycle timing of SRAM.	**07**
Q.4	**(b)**	Explain precharge and equalization circuit for RAM.	**07**
Q.5	**(a)**	Explain these two types of DRAM: 1. Extended data out DRAM (EDO DRAM) 2. Synchronous DRAM	**07**
	(b)	Discuss block diagram of DRAM architecture and write operation of DRAM.	**07**
		OR	
Q.5	**(a)**	In Low power VLSI system design discuss power optimization using operation substitution.	**07**
	(b)	Discuss dynamic supply design for low power VLSI system design.	**07**

****