Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC 2ND Semester Examination – July- 2011

Subject code: X21102

Subject Name: Digital Logic Design

Date:15/07/2011 **Time: 10:30 am – 01:00 pm**

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** What is the function of shift register? With the help of simple diagram explain its working. With block diagram and timing diagram explain the serial transfer of information from register A to register B. **07**

(b) Define : Integrated Circuit and briefly explain SSI, MSI, LSI and VLSI **07**

Q.2 **(a)** Convert the following Numbers as directed: **07**

(i) $(1101.011)_2 = (\quad)_{10}$

(ii) $(266)_{10} = (\quad)_8$

(iii) $(724.63)_{10} = (\quad)_6$

(iv) $(AB6.13)_{16} = (\quad)_2$

(b) Explain with figures how NAND gate and NOR gate can be used as Universal gate. **07**

OR

(b) Explain SOP and POS expression using suitable examples. **07**

Q.3 **(a)** Reduce the expression: **07**

(i) AB + A(B+C) + B(B+C)

(ii) AB + (AC)' + AB'C(AB + C)

(b) Design a 32:1 Multiplexer using four 8:1 Multiplexer and one 4:1 Multiplexer. **07**

OR

Q.3 **(a)** Simplify the Boolean function: **07**

(i) $F(w, x, y) = \sum m(0, 1, 5) + \sum d(4, 7)$

(ii) $F(A,B,C,D) = \sum m(0, 1, 3, 7, 15) + \sum d(2, 11, 12)$

(iii) $F(A,B,C,D) = \Pi M(0, 2, 6, 8, 12) + \Pi d(3, 4, 7, 10, 14)$

(b) What is a Johnson Counter? Explain the working of 4-bit Johnson Counter. **07**

Q.4 **(a)** Design a combinational circuit that converts 4-bit Gray code to 4-bit Binary number using EX-OR gates. **07**

(b) Draw the J-K master-slave flip-flops and explain how to eliminate the race around condition? **07**

OR

Q.4 **(a)** Explain the design of Arithmetic Logic Unit **07**

(b) With simple diagram explain the working of control logic with sequence register and decoder. **07**

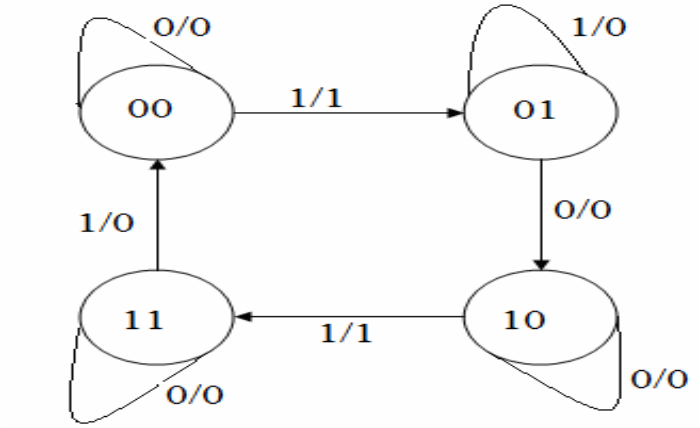
Q.5 **(a)** (i) Demonstrate the De Morgan's theorems using truth tables. **04**

(ii) Implement a two-input exclusive–OR gate using minimum number of NOR gates. **03**

(b) Give classification of Logic Families and Compare CMOS and TTL Families. **07**

OR

Q.5 **(a)** Design the clocked sequential circuit for the given state diagram shown in figure below. **07**



(b) Briefly explain Look-ahead Carry Adder. **07**

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