Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

P.D.D.C. Sem- II Remedial Examination Nov / Dec. 2010

Subject code: X21102 **Subject Name: Digital Logic Design**

Date: 30 / 11/ 2010 **Time: 10.30 am – 01.00 pm**

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Perform the following conversions: (i) $(101101.10101)_2$ to decimal (ii) $(0.65625)_{10}$ to binary (iii) $(6327.4051)_8$ to decimal (iv) $(675.625)_{10}$ to hexadecimal (v) $(11001110001.000101111001)_2$ to hexadecimal (vi) $(396)_{10}$ to BCD (vii) $(3A.2F)_{16}$ to decimal	**07**
	(b)	Perform the following operations: (i) Using 2's complement subtract $(00011)_2$ from $(01100)_2$ (ii) Multiply $(1001)_2$ by $(1101)_2$ (iii) Divide $(1110101)_2$ by $(1001)_2$	**07**
Q.2	**(a)**	Obtain the simplified expressions in sum of products for the following Boolean functions: (i) F(A,B,C,D,E) = Σ (0,2,4,6,9,11,13,15,17,21,25,27,29,31) (ii) F = A′B′C′ + B′CD′ + A′BCD′ + AB′C′	**07**
	(b)	Implement the following Boolean functions (i) F= A (B +CD) +BC′ with NOR gates. (ii) F= (A + B′) (CD + E) with NAND gates.	**07**
		OR	
	(b)	(i) Implement a two-input exclusive–OR gate using minimum number of NAND gates. (ii) Demonstrate the De Morgan's theorems using truth tables.	**07**
Q.3	**(a)**	Discuss 4-bit magnitude comparator in detail.	**07**
	(b)	Design a BCD adder using 4-bit binary adders.	**07**
		OR	
Q.3	**(a)**	Design a BCD-to-decimal decoder.	**07**
	(b)	Implement the following function with a 8:1 multiplexer: F(A,B,C,D) = Σ (0,1,3,4,8,9,15)	**07**
Q.4	**(a)**	Explain the Master-Slave flip-flop.	**07**
	(b)	Design a counter using T flip-flops with the following binary sequence: 0, 1, 3, 7, 6, 4, and repeat.	**07**
		OR	
Q.4	**(a)**	Discuss D-type edge- triggered flip-flop in detail.	**07**
	(b)	Explain the differences between Latch and Flip-flop.	**07**
Q.5	**(a)**	With necessary sketch explain Bidirectional Shift Register with parallel load.	**07**
	(b)	Design a 4-bit up-down binary counter.	**07**
		OR	
Q.5	**(a)**	Design a synchronous BCD counter.	**07**
	(b)	Construct a Johnson counter with ten timing signals.	**07**

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