Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC-Semester –III (May-2012) Examination

Subject code: X31101 **Subject Name: Advance Electronics**

Date: 14/05/2012

Time: 02.30 pm – 05.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw and explain circuit diagram with RC phase shift oscillator.	**07**
	(b)	Explain hybrid π model for single stage CE amplifier configuration.	**07**
Q.2	**(a)**	Enumerate and explain any one method of Digital to Analog conversion.	**07**
	(b)	Draw a circuit diagram of voltage series feedback amplifier. Derive an equation of voltage gain for same.	**07**
		OR	
	(b)	Give the statement of Barkhausen criteria and explain in detail.	**07**
Q.3	**(a)**	Draw and explain circuit diagram of Hartley oscillator.	**07**
	(b)	Draw and explain circuit diagram of RC coupled amplifier with it low frequency response.	**07**
		OR	
Q.3	**(a)**	Derive an equation of f_h for emitter follower circuit at high frequency.	**07**
	(b)	Explain step response of an Amplifier.	**07**
Q.4	**(a)**	Draw and explain circuit diagram of High Threshold Logic NAND gate.	**07**
	(b)	Draw a circuit diagram of current shunt feedback amplifier. Derive an equation of current gain for same.	**07**
		OR	
Q.4	**(a)**	Explain characteristics of operational amplifier.	**07**
	(b)	Draw and explain circuit diagram of TTL NAND gate.	**07**
Q.5	**(a)**	Explain following terms i) CMRR ii) slew rate iii) offset voltage iv)Bias current	**07**
	(b)	List and explain one method of Analog to digital conversion.	**07**
		OR	
Q.5	**(a)**	Explain effect of emitter bypass capacitor on low frequency response for single stage CE amplifier	**07**
	(b)	How offset error voltage can be nullify or minimized? Justify your answer with necessary diagrams/equations	**07**

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