Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER – III • EXAMINATION – WINTER 2012

Subject code: X 31101 Date: 26/12/2012

Subject Name: Advance Electronic

Time: 10.30 am - 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw The Hybrid π model for CE configuration and explain it. Derive the equation for any two parameters those affecting to the transistor at high frequencies for CE configuration	**07**
	(b)	Draw and explain RC coupled amplifier. List all parameters affecting the low frequency response of RC coupled amplifier and derive the equation for any two of them.	**07**
Q.2	**(a)**	Classify the amplifiers based on feedback topology. Explain and draw each with necessary details showing V_i, V_o, R_i, R_o, Ii and I_o.	**07**
	(b)	Obtain the expression for the input and output resistance of an amplifier with current series feedback and comment on the result.	**07**
	(b)	Draw and explain Voltage series feedback. Also derive the expression for input and output resistance.	**07**
Q.3	**(a)**	List out the compensation techniques for stability of amplifiers. Explain with suitable diagram any two of them.	**07**
	(b)	Draw the circuit of RC Phase shift oscillator. Explain the working principle. State the formula for frequency of oscillation.	**07**
		OR	
Q.3	**(a)**	Draw the equivalent circuit of ideal OP-AMP. Briefly describe the important characteristics of the ideal OP-AMP.	**07**
	(b)	If an amplifier has a bandwidth of $200kH_z$ and a voltage gain of 100, what will be the new bandwidth and gain if 5% negative feedback is introduced? What is the product of gain and bandwidth before and after adding negative feedback? What should be the amount of feedback if the bandwidth is restricted to $1MH_z$?	**07**
Q.4	**(a)**	Draw and explain the block diagram of Emitter Coupled Differential Amplifier. Also explain the operation of differential amplifier in the differential mode with suitable diagram.	**07**
	(b)	Draw and explain Hartley Oscillator. Calculate the value of tank circuit capacitor of a Hartley oscillator for $50kH_z$ with L_1 and L_2 are of 100μH.	**07**
		OR	
Q.4	**(a)**	Explain in detail with suitable circuit diagram the following terms: 1) Input bias current and its effect 2. Output offset voltage and its effect	**07**
	(b)	Define CMRR. Explain the significance of CMRR. List out the method to improve the CMRR and explain any one of them.	**07**
Q.5	**(a)**	Explain in detail the Tristate TTL devices. List out the advantages and disadvantages of it. And explain the application of Tristate TTL logic.	**07**
	(b)	List the classification of logical family. Give comparison of them. List out the advantages and disadvantages of each logic families.	**07**
		OR	
Q.5	**(a)**	Explain the operation of Dual Slope ADC and state its advantages.	**07**
	(b)	Define digital to analog converter. List the types of DAC .Draw and explain R-2R DAC.	**07**

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