Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER – VI • EXAMINATION – WINTER 2012

Subject code: X61102 Date: 28/12/2012

Subject Name: VLSI Technology

Time: 10.30 am - 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	State Moore's Law and explain different VLSI Design style in short.	**07**
	(b)	Explain the fabrication steps of nMOS transistor with necessary sketches.	**07**
Q.2	**(a)**	Explain MOSFET CV characteristics with necessary derivation and figures.	**07**
	(b)	Calculate the threshold voltage V_{TO} at VSB = 0 for a polysilicon gate n-channel MOS Transistor, with the following parameters : substrate doping density $N_A = 10^{16}$ cm^{-3}, Polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3}, gate oxide thickness t_{ox} = 500 Å, and oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10}$ cm^{-2} Note that $\varepsilon ox = 3.97\varepsilon 0$, $\varepsilon si = 11.7\ \varepsilon 0$, intrinsic carrier concentration of silicon $n_i = 1.45 \times 10^{10}$ and $\varepsilon 0 = 8.85 \times 10^{-14}$	**07**
		OR	
	(b)	Explain MOSFET capacitance with necessary derivation and figures.	**07**
Q.3	**(a)**	What is scaling? Why it is required? Explain Constant Voltage scaling.	**07**
	(b)	Draw and explain VTC of CMOS Inverter.	**07**
		OR	
Q.3	**(a)**	A CMOS inverter has $V_{TO,n}$ = 0.6 V, $V_{TO,p}$ = - 0.7 V , k_n = 200 μA/V^2 and k_p = 80 μA/V^2. Obtain NM_H and NM_L for V_{DD} = 3.3 V	**07**
	(b)	Draw the Resistive load Inverter circuit diagram. Derive critical voltage points V_{OH}, V_{OL} , V_{IH} and V_{IL} for it.	**07**
Q.4	**(a)**	Explain three stage CMOS ring Oscillator.	**07**
	(b)	Explain NORA CMOS Logic Circuits.	**07**
		OR	
Q.4	**(a)**	Explain on chip clock generation and distribution.	**07**
Q.4	**(b)**	Explain the basic principle of pass transistor circuit. Explain logic "1" transfer and logic "0" transfer.	**07**
Q.5	**(a)**	Explain CMOS Transmission Gate.	**07**
	(b)	Explain Scan based techniques.	**07**
		OR	
Q.5	**(a)**	Give answer of the following question (i) Draw gate level schematic of the clocked NOR- based JK latch and CMOS AOI realization of the JK latch. (ii) Draw CMOS Master- slave D FF.	**07**
	(b)	Draw and explain general architecture of FPGA and CPLD	**07**

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